

Improvement in the Synchronization Process of the Voltage-Sourced Converters Connected to the Grid by PLL in Order to Detect and Block the Double Frequency Disturbance Term

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Abstract

Phase-Locked Loop (PLL) Structures have many applications in power system engineering. When required the synchronous performance of Voltage Sourced Converter (VSC) with Grid, such as wind power generation system, active filters, HVDC transmission lines and FACTS devices, the most common method for accurate estimation of frequency of network, is to use a PLL. However, problems such as grid disturbances due to noise, voltage unbalances, lack of coordination, changes in grid frequency and harmonics can produce a frequency disturbance, twice the grid frequency and disturbed PLL and also the control system connected to it. In this paper, common structures of PLL is introduced. After that, unbalance and disturbance in the three phase input of PLL is studied. Then for idea and invention in PLL, a new control method based on predictive control technique is used in the control strategy of converter. Furthermore, the use of type III controller in PLL to ensure optimal performance in various conditions is proposed in this paper. How to set the parameters of the proposed controller is described by the Bode stability criterion. Conducting simulations to evaluate the performance of the proposed method is done in PSIM software. According to the proposed method and the result observed, the double frequency disturbance term is weakened and also the transient state is improved.

Keywords: Phase-Locked Loop (PLL), Voltage-Sourced Converters (VSC), Synchronization, Current Control, Unbalanced Voltage.

1. Introduction

In order to connect to AC network and inject power by power electronic converters, we require knowing the precise phase angle of voltage. It means that the injected voltage must be in phase with the grid voltage. So it must be synchronized when connected the voltage sourced converter to grid. Here, kind of VSC is grid imposed frequency VSC system. PLL is the mechanism to ensure that the converter is synchronized with grid [1]. So existence of PLL in the converter control system is mandatory.

Current techniques that estimate the frequency are sampled voltage and current. If we consider pure sinusoidal voltage system, by measuring the time between zero crossings of the signal, the frequency can be easily calculated. Furthermore, the wide spread use of power electronics devices in the power generation, transmission, distribution and utilization of electrical energy, has led to change the actual shape of the voltage wave form. Consequently, in practice given signal from power system is associated with noise and distortion, so we need to be able to use more advanced techniques that frequency can be calculated with reasonable

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speed and accuracy. With acceptance of this difficulty, the fact that the behavior of the power system is a flexible system that cannot be predicted accurately, the problem is even more visible. So we need a way to calculate frequency in minimum possible time with maximum accuracy [15].

But when the network is unstable, we have the problem of second harmonic oscillations. The second harmonic oscillations in system, in term of control, the control variables have been second harmonic frequencies and our physical quantities have the second ripple frequency [2,5].

The task of identify and block the negative sequence component is of the equipment named PLL, to determine the phase angle of the voltage source. So when these imbalance conditions occur in the circuit, we face two problems. One must avoid the influence of the negative sequence leading to second harmonic oscillations to grid and another is that we should modify our higher current control strategy.

Classification of different PLLs and also their advantages and disadvantages were illustrated in Table I [15–20]. (T stands for the meaning of "theoretical feasibility" in this case)

This paper is arranged in the following sections: In section 2, the control system of Voltage-Sourced Converters in dq frame are described. In section 3, the common technique for designing controller have been reviewed, In section 4, proposed design guide lines have been studied and control structure of PLL and the position of the proposed control structures has been discussed. In section 5, the results of obtained simulations conducted to evaluate the effectiveness of the proposed model are presented. Section 6 allocated to references.

2. The Control System of Grid Connected Voltage-Sourced Converters [1]

Figure 1 represents a voltage-sourced converter connected to the grid with an overview of its control system. Inverters in distributed generation systems can be utilized in three control forms. Thus the inverters control can be as one of the following three forms [12]:

- 1. Constant Current controlled Voltage-Sourced Inverters (VSI)
- 2. Constant P-V controlled Voltage-Sourced Inverters (VSI)
- 3. Constant P-Q controlled Voltage-Sourced Inverters (VSI)

In this paper, the type of current control is constant power (active and reactive). As can be seen, control in these converters is in a rotating reference frame (dq frame) rotating with angular speed of w_0 and we have the following:

	Design Simplicity	Frequency adaptive & range	Distortion insensitivity	Unbalance insensitivity
SF-PLL	Good	Average	Average	Poor
PQ-PLL	Average	Average	Average	Poor
DSF-PLL	Average	Average	Good	Good
SSI-PLL	Average	Average	Good	Good
DSOGI-PLL	Average	Average	Good	Good
EPLL	Average	Average	Good	Good
3MPLL	Average	Average	Good	Good
Q-PLL	Average	Average	Good	Т
RPLL	Average	Average	Good	Т
PPLL	Average	Good	Good	Good
ALC-PLL	Average	Average	Good	Т
MR-PLL	Average	Average	Good	Т
APLL	Average	Average	Good	Good
ZCD	Good	Poor	Poor	Poor
SV	Average	Poor	Average	Poor
WLSE	Average	Average	Good	Good

 Table I.
 Selection guidance for specific applications [4]

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Figure 1. Schematic diagram of a current-controlled real/reactive power controller in dq-frame.

$$\omega = \frac{d\rho}{dt} \tag{1}$$

Suppose that balanced AC system voltage is defined as:

$$\begin{cases} V_{sa}(t) = \hat{V}_{s} \cos\left(\omega_{0}t + \theta_{0}\right) \\ V_{sb}(t) = \hat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{2\pi}{3}\right) \\ V_{sc}(t) = \hat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{4\pi}{3}\right) \end{cases}$$
(2)

Then after the dynamic equations reflect the performance of the AC converter, Figure 1, in the reference frame we have:

$$L\frac{di_d}{dt} = L\omega(t)i_q - (R + r_{on})i_d + V_{td} - V_{sd}$$
(3)

$$L\frac{di_q}{dt} = -L\omega(t)i_d - (R + r_{on})i_q + V_{tq} - V_{sq}$$
(4)

$$\frac{d\rho}{dt} = \omega(t) \tag{5}$$

$$V_{sd} = \widehat{V}_s \cos\left(\omega_0 t + \theta_0 - \rho\right) \tag{6}$$

$$V_{sq} = \widehat{V}_s \sin\left(\omega_0 t + \theta_0 - \rho\right) \tag{7}$$

Active and reactive power exchange with the grid is defined as follows:

$$P_{s}(t) = \frac{3}{2} \Big[V_{sd}(t) \, i_{d}(t) + V_{sq}(t) \, i_{q}(t) \, \Big], \tag{8}$$

$$Q_{s}(t) = \frac{3}{2} \Big[-V_{sd}(t) \, i_{q}(t) + V_{sq}(t) \, i_{d}(t) \, \Big], \tag{9}$$

Basically, the obvious advantage of transferring data to the rotating reference frame is dependent upon the choice of dq frame speed. If $\omega = \omega_0$ and $\rho(t) = \omega_0 t + \theta_0$, then $V_{sq} = 0$ and V_{sd} will be equal to voltage amplitude. In this case values of all variables in dq frame $(i_q, i_q, ...)$ are DC component in steady state and to achieve the desired response, we can utilize the ordinary PI controllers in control structures of these converters. The control mechanism which ensures simultaneously that $\rho(t) = \omega_0 t + \theta_0$ is known as Phase Locked Loop or PLL. In this case because the angular speed of dq frame is the same as the grid frequency, it is called Synchronous Reference Frame (SRF). Then the possibility of controlling the active power of converter by the q component is made.

$$P_{s}(t) = \frac{3}{2} V_{sd}(t) i_{d}(t)$$
(10)

$$Q_{s}(t) = -\frac{3}{2} V_{sd}(t) i_{q}(t)$$
(11)

Appropriate response of the converter control system or in other words to track the reference value of active and reactive power, largely dependent to appropriate application of PLL accurate estimation of frequency and voltage phase angle. Therefore the appropriate design of different blocks of this loop and evaluation of its performance is vital.

3. Proposed Type-4 PLL

3.1 Compensator Design in Order to have the Zero Steady State Error for All Different Inputs

In this section, different approaches to design a PLL are investigated [6–10]. And then the proposed idea is illustrated. In each case, the general structure is presented and its advantages and limitations are briefly discussed.

Figure 2 (a) illustrates the basic scheme of a conventional SRF-PLL, in which LF(s) is the LF transfer function. Supposing that, the three phase input voltages are balanced and undistorted, the small signal model of the SRF-PLL can be obtained as shown in Figure 2 (b), where θ and $\hat{\theta}$ are the input and estimated phases, respectively. θ_e is the phase error, and V is the input voltage amplitude. It is



Figure 2. a) Basic scheme of a conventional SRF-PLL b) Its small signal model.

shown in [7, 8, 11] that, considering the LF as a proportional-integral (PI) controller (i.e., $LF(s) = K_p + \frac{K_i}{s}$ where K_p and K_i are the proportional and integral gains, respectively) results in a type-2 PLL.

The question is: what form of *LF*(*s*) is required to realize a type-3 PLL? It is known that, the type-3 PLLs are able to track a frequency ramp input with zero steady state phase error. So to realized a type-3 PLL, *LF*(*s*) should be designed such that, for $\theta(s) = \frac{\Delta \dot{\omega}}{S^3}$, where $\Delta \dot{\omega}$ is the frequency ramp rate in $\frac{rad}{s^2}$ we obtain $\lim_{t\to\infty} \theta_e(t) = 0$.

From Figure 2 (b) the phase error Laplace transform in response to a frequency ramp input is:

$$\theta_e(s) = \frac{s}{s + LF(s)V} \theta(s) = \frac{1}{s^2} \frac{\Delta \dot{\omega}}{s + LF(s)V}$$
(12)

Applying the final value theorem to (12), yields the steady state phase error, θ_{ess} , as

$$\theta_{e,ss} = \lim_{t \to +\infty} \theta_e(t) = \lim_{s \to 0} s \theta_e(s) = \lim_{s \to 0} \frac{1}{s} \frac{\Delta \dot{\omega}}{s + LF(s)V} \quad (13)$$

For $\theta_{e,s}$ to be zero, it is required that, LF have a transfer function as $LF(s) = \frac{n(s)}{s^2}$, $n(0) \neq 0$, where n(s) is a polynomial of order smaller than or equal to 2. Based on this, the open loop transfer function can be obtained from Figure 2 (b) as:

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta_{e}(s)} = V \times LF(s)\frac{1}{s} = \frac{n(s)V}{s^{3}}$$
(1)

From (14), it is obvious that the asymptotic plot of $G_{ol}(s)$ has a phase of -270° at zero frequency and a slope of $-60 \frac{dB}{dec}$ at low frequency. Therefore to stabilize the system, the LF must have a pair of zeros before the gain crossover frequency ω_c . Notice that presence of two zeros before ω_c break the asymptotic slope to $-20 \frac{dB}{dec}$ and push the phase up to 180° of negative phase and consequently stabilize the system. So to realize a type-3 PLL, the LF transfer function should be of the form:

$$LF(s) = \frac{n(s)}{s^2} = \frac{c_{n2}s^2 + c_{n1}s + c_{n0}}{s^2}$$
(15)

where c_{n0} , c_{n1} , c_{n2} are non-zero positive constants.

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Based on Figure 2 (b) and considering the LF transfer function as that given in (4), the characteristic polynomial of the type-3 SRF-PLL can be obtained as

$${}^{3} + Vc_{n2}s^{2} + Vc_{n1}s + Vc_{n0} = 0$$
(16)

Applying the Routh-Hurwitz stability criterion to (16) yields:

$$V > \frac{c_{n0}}{c_{n1}c_{n2}}$$
(17)

which means to ensure the stability, the input voltage amplitude should be greater than $c_{n0}/(c_{n1}c_{n2})$. so the possibility of instability under severe voltage sags or faults is a serious drawback associated with the type-3 SRF-PLL. And it has a constant phase error under frequency parabolic input.

Now, Another question is: what form of LF(s) is required to realize a type-4 PLL? It is known that, the type-4 PLLs are able to track a frequency parabolic input with zero steady state phase error.

So to realize a type-4 PLL, *LF*(*s*) should be designed such that, for $\theta(s) = \frac{\Delta \dot{\omega}}{s^4}$, where $\Delta \dot{\omega}$ is the frequency parabolic rate in $\frac{rad}{s^3}$, we obtain $\lim_{t \to \infty} \theta_e(t) = 0$.

From Figure 2 (b), the phase error Laplace transform in response to a frequency parabolic input is:

$$\theta_{e}(s) = \theta - \bar{\theta} = \theta - \frac{VLF(s)\theta}{s + VLF(s)} = \frac{s\theta(s)}{s + VLF(s)} = \frac{1}{s^{3}} \frac{\Delta\dot{\omega}}{s + VLF(s)}$$
(18)

Applying the final value theorem to (18), yields the steady (14) state phase error, θ_{ess} as: $\boldsymbol{4944}$

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$$\theta_{e,ss} = \lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} s \theta_e(s) = \lim_{s \to 0} \frac{1}{s^2} \frac{\Delta \dot{\omega}}{s + LF(s)V}$$
(19)

For $\theta_{e,ss}$ to be zero, it is required that LF have a transfer function as one of the three following functions:

$$LF(s) = \frac{k_{p}s + k_{i}}{s} \frac{s^{2} + (2\omega)^{2}}{(s + \omega_{p})^{2}}$$
(20)

$$LF(s) = \frac{k_{p}s + k_{i}}{s} \frac{s^{2} + (2\omega)^{2}}{s^{2} + 2\zeta\omega_{n}s + \omega_{n}^{2}}$$
(21)

$$LF(s) = \frac{k_p s + k_i}{s} \frac{s^2 + (2\omega)^2}{s^2 + \omega_p^2}$$
(22)

For compare and contrast, different kinds of Loop filter are as follows:

Type of PLL	Kind of loop filter
Type-2	$LF(s) = \frac{k_p s + k_i}{s}$
Type-3	$LF(s) = \frac{\omega_n^2}{s^2 + 2\zeta \omega_n s}$
Type-4	$LF(s) = \frac{k_{p}s + k_{i}}{s} \frac{s^{2} + (2\omega)^{2}}{(s + \omega_{p})^{2}}$
	$LF(s) = \frac{k_{p}s + k_{i}}{s} \frac{s^{2} + (2\omega)^{2}}{s^{2} + 2\zeta \ \omega_{n}s + \omega_{n}^{2}}$
	$LF(s) = \frac{k_{p}s + k_{i}}{s} \frac{s^{2} + (2\omega)^{2}}{s^{2} + \omega_{p}^{2}}$

Table II provides a comparison between the type-2, type-3 and type-4 SRF-PLL in terms of the steady-state phase-error for different types of inputs.

3.2 Compensator Design in Order to Block the Double Frequency Disturbance Term

There are many different methods for designing the PI-regulator gains K_p and τ which method is the most suitable depends on the criteria of the regulator. Dynamic performance of the PLL is highly influenced by the compensator H(s). Consider the block diagram of Figure 3 indicating that the reference signal, $\omega_0 t + \theta_0$, is composed of a constant component, that is, θ_0 , and a ramp function, that is, $\omega_0 t$. Since the loop gain includes an integral term, ρ tracks the constant component of the reference signal with zero steady-state error. However, to ensure a zero steady-state error for the ramp component, the loop gain must include

Table II. Steady state error for different inputs

Input	Type-2 SRF-PLL	Type-3 SRF-PLL	Type-4 SRF-PLL
Phase step	0	0	0
Frequency step	0	0	0
Frequency ramp	Cte.	0	0
Frequency parabolic	Cte.	Cte.	0



Figure 3. Control block diagram of the PLL.

at least two integrators. Therefore, H(s) must include at least one integral term, that is, one pole at s=0. The other poles and zeros of H(s) are determined mainly on the basis of the closed-loop bandwidth of the PLL and stability indices such as phase margin and gain margin.

Unbalanced voltages and harmonic distortions in PLL input is an inevitable matter. This unbalance and different harmonics can cause disfunction in PLL performance. In general, equation (12) is used to display input three phase voltages of PLL. In this equation, assume that V_{sabc} represents an unbalanced voltage with a negative-sequence fundamental component and a fifth-order harmonic component [14, 16], as:

$$V_{sa}(t) = \widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0}\right) + k_{1}\widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0}\right) + k_{5}\widehat{V}_{s} \cos\left(5\omega_{0}t + \theta_{5}\right)$$

$$V_{sb}(t) = \widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{2\pi}{3}\right) + k_{1}\widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{4\pi}{3}\right) + k_{5}\widehat{V}_{s} \cos\left(5\omega_{0}t + \theta_{5} - \frac{4\pi}{3}\right)$$

$$V_{sc}(t) = \widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{4\pi}{3}\right) + k_{1}\widehat{V}_{s} \cos\left(\omega_{0}t + \theta_{0} - \frac{2\pi}{3}\right) + k_{5}\widehat{V}_{s} \cos\left(5\omega_{0}t + \theta_{5} - \frac{2\pi}{3}\right)$$

$$(23)$$

where, k_1 and k_5 are the amplitude of the negative-sequence (fundamental) and fifth order harmonic components, respectively, relative to the amplitude of the positive



Figure 4. A) Schematic diagram of the PLL. B) Basic structure of PLL.

sequence (fundamental) component. The space phasor corresponding to V_{sale} is:

$$\vec{V}_{s} = \widehat{V}_{s}e^{j(\omega_{0}t+\theta_{0})} + K_{1}\widehat{V}_{s}e^{-j(\omega_{0}t+\theta_{0})} + K_{5}\widehat{V}_{s}e^{-j(5\omega_{0}t+\phi_{5})}$$
(24)

If the PLL of Figure 4(a) is under a steady-state operating condition, that is, $\rho = \omega_0 t + \theta_0$, then based on Park transformation V_{sd} and V_{sg} are:

$$V_{sd} = \widehat{V}_s + K_1 \widehat{V}_s \cos\left(2\omega_0 t + 2\theta_0\right) + K_5 \widehat{V}_s \cos\left(6\omega_0 t + \theta_0 + \phi_5\right)$$
(25)
$$V_{sq} = -K_1 \widehat{V}_s \sin\left(2\omega_0 t + 2\theta_0\right) - K_5 \widehat{V}_s \sin\left(6\omega_0 t + \theta_0 + \phi_5\right)$$
(26)

Equations (19) and (20) indicates that, in addition to DC component, V_{sd} and V_{sq} include sinusoidal components with frequencies $2\omega_0$ and $6\omega_0$.

The basic structure of a Phase-locked loop (PLL) is shown in Figure 4(b). It consists of three fundamental blocks:

- 1. The phase detector (PD): This block generates an output signal proportional to the phase difference between the input signal, v, and the signal generated by the internal oscillator of the PLL, \dot{v} . Depending on the type of PD, high frequency AC components appear together with the DC phase angle difference signal.
- The loop filter (LF): This block presents a low pass filtering characteristics to attenuate the high frequency AC components from the PD output. Typically, this block is constituted by a first-order low pass filter or a PI controller.
- 3. The voltage controlled oscillator (VCO): This block generates at its output an AC signal whose frequency is



Figure 5. Response of the PLL to a sudden AC system voltage imbalance [1, 13].

shifted with respect to a given central frequency, ω_c , as a function of the input voltage provided by the LF.

Since during a fault, an unbalance in grid voltage is created, so *d* and *q* axis component are generated in the PLL input. This negative sequence cause a frequency twice the grid frequency in V_{sd} and V_{sq} (Figure 5). So the closest undesirable frequency that is established in PLL and should be removed is twice the grid frequency. Since, only DC part of V_d and V_q components is needed to extract the frequency and phase, the closed loop characteristics (H(s)) should be a low pass filter.

(Because V_d and V_q components are normally DC values (i.e. with zero frequency) we should use the low pass filter with high gain in low frequencies.)

Another problem is that in equation (17), we must inquire how much is the size of k_1 in normal mode or it is how many percent of the fundamental component. This Improvement in the Synchronization Process of the Voltage-Sourced Converters Connected to the Grid by PLL in Order to Detect and Block the Double Frequency Disturbance Term

value is how much in a state of unbalance? And to what extent it is harmful to the performance of PLL?

According to literature (various references), the amplitude of the negative sequence in normal mode of grid is $k_1 = 0.01$, that in unbalance condition, this value reach to $k_1 = 0.5$ or fifty percent of the fundamental component. In order not to disrupt the PLL, this value should be reach to 0.01. So closed loop gain in this frequency must be a value to set k_1 to 0.01. (Table III)

When the negative sequence component is created, the amplitude of this component must be blocked. Maximum amplitude is fifty percent of the main component.

In Normal mode operation this component is exist, but in this case amplitude is equal to 0.01 range of the fundamental component. (Figure 6)

To solve the problem of double frequency disturbance term, we use the type-3 controller. Existence of integral term in controller is an evidence to increase gain at low frequencies which makes the Bode diagram decrease with slope of $-20 \frac{dB}{dec}$. This controller increased the frequency of the desired phase so that phase margin is increased. Moreover, the controller has a good roll-off rate at high frequencies.

3.3 Improved Compensator Design Proposed for PLL

In general, the type-3 compensator transfer function for Figure 3 is as follows:

$$G_{type3} = K \frac{\left(\frac{s}{\omega_z} + 1\right)^2}{s\left(\frac{s}{\omega_p} + 1\right)^2}$$
(27)

In continue, the controller coefficients (*K*, ω_z , ω_p) can be obtained as follows:

A Bode diagram of overall shape of the open loop system with the controller is as follows:

As clearly shown in Figure 7, because the number of poles of the system and controller $(G_{type3} \times \frac{1}{s})$ is two more than the zeros of the system and controller, we have a line with negative slope of $-40 \frac{dB}{dec}$ at high frequencies in Bode diagram. So we get interpretation of the cut off frequency (ω_c).

The first and smallest frequency that we will not want to appear in the output is 120 *Hz*, that should remove (filter) the frequencies more than 120 *Hz*.

As mentioned above, in normal state k_1 =0.01 and in unbalanced condition it reaches to 0.5. So, the closed



Figure 6. Minimum and maximum value of V_d and V_q axis [3].

 Table III.
 Display Voltage in Different Sequences [3]

Voltage	Phase A	Phase B	Phase C
Fundamental amplitude = V_1	sin <i>w</i> t	$\sin\left(\omega t - \frac{2\pi}{3}\right)$	$\sin\!\left(\omega t + \frac{2\pi}{3}\right)$
Negative- sequence amplitude = 0.01 V.	sin <i>cot</i>	$\sin\!\left(\omega t - \frac{2\pi}{3}\right)$	$\sin\!\left(\omega t - \frac{2\pi}{3}\right)$
5th harmonic amplitude = $0.025 V_1$	$\sin(5\omega t + \phi)$	$\sin\left(5\omega t + \frac{2\pi}{3} + \phi\right)$	$\sin\left(5\omega t - \frac{2\pi}{3} + \phi\right)$

loop gain of the system (by controller) must be determined so that gain in f=120 Hz reached 0.01. To obtain the attenuation coefficient that it is not affected PLL, the attenuation in wave form in 120 Hz is calculated as:

$$\alpha \times 0.5 = 0.01 \rightarrow \alpha = \frac{0.01}{0.5} = \frac{1}{50} = \frac{2}{100}$$
 (28)

$$20\log\left(\frac{2}{100}\right) = -33.97 \approx -34dB$$
 (29)

 α is the gain of the system at f = 120 Hz. α is created -34 dB attenuation at f = 120 Hz.

According to the line equation, $(y-y_0=m(x-x_0))$ and at one point $(-34 \, dB, 120 \, Hz)$ and the slope $-40 \frac{dB}{dec}$, we get out of here ω_c . ω_c or transition frequency of interest is where the diagram breaks the $0 \, dB$ axis. (Note that transition



Figure 7. Bode diagram [9].



Figure 8. Bode Diagram of the open loop system- the display of attenuation.

frequency or cut off frequency is in which the system gain (the size of the open loop transfer function) is equal to 1, or in other words, when we equalize |GH| = 1 = 0 dB, the obtained frequency is the cut off frequency.

$$|GH| = 1 \rightarrow \omega_{\sigma} = cut \ off \ frequency$$
 (30)

In fact, ω_p that is the place of changing slope to $-40 \frac{dB}{dec}$ in Bode diagram, should selected before $\omega_c(2\pi \times 120 Hz)$ to create high frequency attenuation.

Zeros should be nearly close to the origin and long before ω_p . We consider line equation in format of equations:

$$G_{(dB)} = m_{\left(\frac{dB}{dec}\right)}\omega_{(dec)} + c \tag{31}$$

for
$$f = 120 \rightarrow G_{(dB)} = -34$$
 (32)

$$\log 120 = 2.07 \to -34 = -40 \times 2.07 + c \to c = 48.8 \ dB \tag{33}$$

In general, line equations having a slope and one point is as follows:

$$G_{(dB)} = -40\omega_{(dec)} + 48.88 \tag{34}$$

Now we want to find ω_c where the Bode diagram, crosses the 0 *dB* axis.

$$0 = -40\omega + c \to \omega = \frac{48.8}{40} = 1.22 \ dec \tag{35}$$

In the above equations, ω_c is of *log f*, so now we make the inverse logarithm.

$$f = 10^x = 16.6 \ Hz$$
 (36)

$$\omega_c = 2\pi f = 104 \frac{rad}{s} \tag{37}$$

equency, so $\omega_p = 75$ and $\omega_z = 6.5$ is selected.

As mentioned above, the nature of controller is so that poles should be enough before zeros, in order to compensate droop frequency, so $\omega_p = 75$ and $\omega_z = 6.5$ is selected.

Now, to calculate the last parameter, (k), the size of the closed loop transfer function equalized to 1 or 0 dB. *K* is calculated as follows:

$$\begin{vmatrix} G_{type III} G_p \\ \\ \\ = 1 \rightarrow K \left| \frac{\left(1 + \frac{j\omega_c}{2\pi f_z} \right)^2}{j\omega_c \left(1 + \frac{j\omega_c}{2\pi f_\rho} \right)^2} \right| \times |G_p| \\ \\ \\ = 1 \rightarrow k \approx 75$$

$$(38)$$

As a result, corresponding controller is obtained according to equation (16) as follows:

$$H(s) = \frac{4.264 \times 10^5 s^2 + 5.35 \times 10^6 s + 1.683 \times 10^7}{39.48 s^3 + 5953 s^2 + 2.244 \times 10^5 s}$$
(39)

Finally, the ultimate designed diagram of open loop control system is which indicates the frequencies of how much attenuation is been plotted in Figure 9 (a. Magnitude/ Frequency).

The following results are obtained from the open loop bode diagram.

As observed in the bode diagram of first Figure of Figure 9 from the stability characteristics of the bode diagram we find the close loop is stable. In cut off frequency, $f_c = 11.5 Hz$, phase margin, $PM = 82.6^{\circ}$. In addition, the amount of attenuation is -34.6 dB in 120 Hz.

The closed loop characteristic is obtained as follows:

As it is shown in the frequency response of the closed loop system, bandwidth is $\omega_{_{3dB}} = 15.9 Hz$.

In these conditions, the use of a type-3 compensator (type-3 controller) as H(s) is recommended for the following reasons:

This compensation have one pole on origin and 2 poles and 2 zeros with selective places. Because of origin pole, it can improve the regulation and can also increase phase to 90 degree Improvement in the Synchronization Process of the Voltage-Sourced Converters Connected to the Grid by PLL in Order to Detect and Block the Double Frequency Disturbance Term



Figure 9. Frequency response of the open loop system with proposed compensators.

Table IV. Results	
Phase Margin	$P.M. = 82.6^2$
Cut-off frequency	$\omega_g = 11.5 Hz$

at a selected frequency. So it can increase cut-off frequency and bandwidth to get faster the response speed of system.

In next section, the simulation results confirmed the calculated controller, the symmetrical short circuit is simulated and tested on different conditions.

4. Simulation Results

Due to type-3 controller presented in last section and equations obtained in this way, all simulations using type-3 and predictive controllers have been presented. Simulations were carried out in Figure 12. Figure 12 To Figure 15 by PSIM software and plotted in MATLAB software. In this section, the following simulation results will be presented.

- 1. Evaluation of system behavior during start-up.
- 2. Evaluation of system behavior during voltage unbalance in three phase system.
- 3. Evaluation of system behavior when changing frequency.
- 4. Evaluation of dynamic behavior of system in response to step changes in the reference frame of the active and reactive power.

4.1 Single Line Diagram of the Studied System

Single line diagram of the power system is given in Figure 11.

4.2 Introducing the Studied System

Simulations were carried out on studied system of Figure 11 with parameters of Table V. The studied system is consisting of a three phase voltage-sourced converter that



Figure 10. Frequency response of the closed loop system with proposed compensations.



Figure 11. Structure of the studied network, three phase PWM voltage-sourced converter connected to grid, a) three phase power circuit, b) Single phase equivalent circuit.

is connected to an infinite bus through a filter and dq reference frame is used in its control strategy.

4.3 PLL Behavior on Start-up

Figure 12 illustrates the start-up transient of the PLL with proposed controller. As shown in Figure 12 in t = 0.05 sec transient time is finished, f = 60 Hz and also V_{sa} remains on zero.

4.4 PLL Behavior During Voltage Unbalance in Three Phase System

Figure 13 illustrates the dynamic response of the PLL to a sudden imbalance in V_{sabc} . Initially, the PLL is in a steady state. At t = 0.25 sec, the AC system voltage V_{sabc} becomes unbalanced such that V_{sa} undergo step changes, from 391 to 260 V, and at t = 0.35 sec, V_{sabc} reverts to its balanced pre disturbance condition. Figure 13 shows that V_{sq} have a average DC value at zero. It also shows that V_{sd} and V_{sq} includes a 120-Hz sinusoidal

Quantity	Symbol (Dimension	n) Parameter
	Inverter Parameters	;
$V_{_{DC}} = 1250 V$	$V_{_{DC}}(V)$	Input DC link voltage
$f_s = 3420 \ Hz$	f_s (Hz)	Sampling frequency (Switching frequency)
$r_{_{on}} = 0.88 \ m\Omega$	$r_{_{on}}(m\Omega)$	Resistor
	Filter Parameters	
$L = 100 \ \mu H$	L (µH)	Filter Inductance
$R = 0.75 \ m\Omega$	$R(m\Omega)$	Filter equivalent resistance
	Grid parameters (Power s	ystem)
$\omega_0 = 377 \ rad/s$	$\omega_{_0}(rad/s)$	Grid frequency
$V_{L} = 480 V$	$V_{_L}(V)$	Line-to-line rms voltage
$V_{sd} = \sqrt{2} \times \frac{480}{\sqrt{3}} \approx 391V$	$V_{_{sd}}\left(V ight)$	Voltage Amplitude
$V_{d} = 1.0 V$	$V_{d}(V)$	Steady state d-axis voltage (p.u.)
	Control system parameters (Con	ntrol circuit)
$\tau_i = 10 \times \frac{1}{f_s} = 10 \times T = \frac{1}{3420} \times 10 =$	$0.02 = 2 ms \tau_i(ms)$	Time constant
$\begin{array}{c} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	(c)	(0) (1)
	(d)	400 300 200 200 200 200 200 200 200 200 2

Table V. Information of inverter, inter, network and control	Tab	le	V.	Information	of inverter.	filter.	network a	nd controlle
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Figure 12. Start-up response of the PLL.

ţ

0.06

0.1 time (s) 0.16 0.18

0.14

-10

0.02

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Figure 13. Response of the PLL to a sudden AC system voltage unbalance.

ripple due to the negative sequence component of V_{sabc} but this double frequency disturbance term was weakened in V_{sq} than V_{cd} .

4.5 PLL Behavior When Changing Frequency

Figure 14 depicts the dynamic response of the PLL to two stepwise changes in ω_0 , the first one from $2\pi \times 60 = 377 \ rad/s$ to $2\pi \times 63 = 396 \ rad/s$ at $t = 0.25 \ sec$, and the other from $396 \ rad/s$ to $2\pi \times 57 = 358 \ rad/s$ at $t = 0.3 \ sec$.

Figure 14. Response of the PLL to a sudden AC system frequency change.

4.6 Evaluation of Dynamic Behavior of System in Response to Step Changes in the Reference Frame of the Active and Reactive Power

In this section, the studied system is subjected to the following sequence of events: until t = 0.05 s, the gating pulses are blocked and the controllers are inactive. This permits the PLL to reach its steady state. At t = 0.15 s the gating pulses are unblocked and the controllers are activated,



Figure 15. Dynamic response of real and reactive power.

while $P_{sref} = Q_{sref} = 0$. At t = 0.20 s, P_{sref} is subjected to a step change from 0 to 2.5 *MW*. At t = 0.30 s, P_{sref} is subjected to another step change from 2.5 to -2.5 MW. At t = 0.35 s, Q_{sref} is subjected to a step change from 0 to 1.0 *MVAR*.

5. Conclusion

In this article as an idea and innovation, we use a new predictive controller named Deadbeat in control circuit of PWM voltage sourced converter and a type-3 controller was used as Loop filter in PLL control circuit and the simulations were performed. Results were shown that the proposed controller is more sensitive to the problem. In the proposed method, in addition to weaken the double frequency disturbance term, in practice it is very easy to implement. In addition simulations were performed on the change of grid frequency. Simulation results confirm the good performance of the proposed method.

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